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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314

EXAMINER	
GOMA, TAWFIK A	
ART UNIT	PAPER NUMBER
2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,779	SU ET AL.	
	Examiner	Art Unit	
	Tawfik Goma	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-17 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, 5-17 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the amendment filed on 1/29/2007.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-14, 16 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishiwata et al (US 6792013).

Regarding claim 9, Ishiwata discloses a method for controlling a data write operation in an optical storage system including an operational amplifier having a positive input end, a negative input end and an output end for outputting a write-control signal at the output end (fig. 3 and col. 1 lines 17-23), the operational amplifier being operated in one of a short-term mode, a long-term mode and a closed-loop mode (figs. 2-4), comprising the steps of: executing a short-term mode for initializing a write-control signal by using virtually grounding effect (col. 7 lines 55-63 and fig. 4); executing a long-term mode for charging the write-control signal by using virtually grounding effect (col. 8 lines 1-19 and fig. 4), with which the output end of the operational amplifier is coupled to the negative input end thereof and the positive input end of the operational amplifier couples to a voltage level used for recording data onto a compact disk for charging the write-control signal (C2 = 1, fig. 3 and Initiation, fig. 4) such that the positive input end and the negative input end of the operational amplifier are virutually grounded (col. 8

lines 1-19, figs. 3 and 4); and executing the closed-loop mode for employing the charged write-control signal for recording data onto a compact disk (col. 8 lines 47-64). The virtual ground effect is exhibited by the nature of an opamp to have no current flowing into it's terminals, effectively creating a V+=V- terminal effect which is a property of opamps. See response to arguments below for further explanation.

Regarding claim 10, Ishiwata further discloses a step of initializing the write-control signal within the short-term mode (col. 7 lines 55-63).

Regarding claim 11, Ishiwata further discloses further a step of using a digital to analog control signal to control the charging operation of the write-control signal (6, 8 , fig. 3).

Regarding claim 12, Ishiwata further discloses wherein in the closed-loop mode, the write-control signal is used for controlling the recording operation (figs. 3,4 and col. 9 lines 1-32).

Regarding claim 13, Ishiwata further discloses a step of re-executing the long-term mode after the recording operation for re-initializing the write-control signal (write, read, write, fig. 4).

Regarding claim 14, Ishiwata further disclose a step of using a first time period control signal, a second time period control signal and a third time period control signal for controlling the operational amplifier to be operated in the short-term mode, the long-term mode and the closed-loop mode, in which the first and second time period control signals are switched between a first level and a second level (C0-C4, fig. 3 and col. 7 lines 18-32).

Regarding claim 16, Ishiwata further discloses wherein the operational amplifier has a positive input end, a negative input end and an output end, and the output end of the operational amplifier serves for outputting the write-control signal (4, fig. 3).

Regarding claim 22, Ishiwata further discloses wherein the long-term mode is executed again after the writing operation for reinitializing the write-control signal (fig. 4 and col. 8 lines 1-19).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwata et al (US 6792013) in view of Inaba et al (US 5477557).

Regarding claims 20-21 Ishiwata fails to disclose a sampling and holding circuit and a gain amplifier, in which the sampling and holding circuit receives the feedback control signal and the feedback control signal is amplified by the gain amplifier, and the feedback control signal is amplified before being sent to the negative input end of the operational amplifier. In the same field of endeavor, Inaba discloses a laser drive circuit wherein a feedback signal is provided to the driving amplifier circuit through a gain amplifier and a sample and hold circuit (fig. 6). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the device disclosed by Iswhiwata by providing a gain amplifier

and sample and hold circuit as taught by Inaba. The rationale is as follows: One of ordinary skill in the art at the time of the applicant's invention would have been motivated to provide a gain amplifier and sample and hold circuits in order to a stable and detectable feedback signal from the photo-detector.

Claims 1-2, 5, 8, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwata et al (US 6792013) in view of Dosho et al (US 5822236).

Regarding claim 1, Ishiwata discloses an apparatus for controlling a data write operation in an optical storage system comprising an operational amplifier having a positive input end, a negative input end and an output end for outputting a write-control signal at the output end (fig. 3 and col. 1 lines 17-23), the operational amplifier being operated in one of a short-term mode, a long-term mode and a closed-loop mode (figs. 2-4); wherein in the long-term mode, the operational amplifier charges the write-control signal (Initiation, figs. 2 and 4), the output end of the operational amplifier is coupled to the negative input end thereof and the positive input end of the operational amplifier couples to a voltage level used for recording data onto a compact disk for charging the write-control signal (C2 = 1, fig. 3 and Initiation, fig. 4) such that the positive input end and the negative input end of the operational amplifier are virtually grounded (V+=V- characteristic of opamps); and in the closed-loop mode, the charged write-control signal is employed to record data on a CD (Steady, figs. 2 and 4). Ishiwata fails to disclose wherein in short-term mode, the operational amplifier is formed as a voltage follower for initializing the write-control signal. Ishiwata does disclose that the write control signal is initiated to 0V prior to the write mode being initiated (WLD, fig. 4) and that the circuit is not limited to the switching operations disclosed (col. 10 lines 48-53). In the same field of

endeavor, Dosho discloses a read/write device for a memory in which a reset mode (short-term mode) is used prior to reading/writing and that the reset configuration is a voltage follower (figs. 3 (b) and 32, fig. 4). It would have been obvious to one of ordinary skill in the art to modify the apparatus disclosed by Ishiwata by providing a reset mode as taught by Dosho. The rationale is as follows: One of ordinary skill in the art at the time of the applicant's invention would have been motivated to provide a short-term or reset mode in order to discharge any remaining parasitic charge in the capacitor (Dosho abstract).

Regarding claims 2, Dosho further discloses wherein in the short-term mode, the positive input end of the operational amplifier is coupled to a reference voltage, and the negative input end thereof is coupled to the output end for forming a voltage follower so as to initialize the write-control signal (3, fig. 4).

Regarding claim 5, Ishiwata further discloses wherein in the long-term mode, the operational amplifier charges the write-control signal to the voltage level used for recording data onto the compact disk (Initiation, fig. 4 and col. 8 lines 1-19).

Regarding claim 8, Dosho further discloses wherein when the writing operation is completed, the short-term mode is actuated again so as to initialize the write-control signal again (fig. 1b).

Regarding claim 15, Ishiwata discloses a read/write device used in an optical storage system comprising (fig. 3): a read-control device for generating a read-control signal in response to a feedback control signal (31, fig. 3); a write-control device having an operational amplifier for generating a write-control signal in response to the feedback control signal (11, fig. 3), wherein the operational amplifier is formed for initializing the write-control signal when

being operated in a short-term mode (col. 7 lines 55-63); the operational amplifier charges the write-control signal in advance when being operated in a long-term mode (Initiation, fig. 4),), the output end of the operational amplifier is coupled to the negative input end thereof and the positive input end of the operational amplifier couples to a voltage level used for recording data onto a compact disk for charging the write-control signal (C2 = 1, fig. 3 and Initiation, fig. 4) such that the positive input end and the negative input end of the operational amplifier are virtually grounded (V+=V- characteristic of opamps); the charged write-control signal is used to control an operation of recording data onto a compact disk when the operational amplifier is operated in a closed-loop mode(fig. 4 and col. 9 lines 11-31); and a read/write head for generating a laser beam in response to the read-control signals, the write-control signals, a read-enable signal, and a write-enable signal (1, 5, fig. 3), wherein the read/write head generates a feedback signal based on the laser beam for being fed back to the read-control device and the write-control device (2, fig. 3). Ishiwata fails to disclose a voltage follower configuration for the short-term mode but Dosho discloses the voltage follower for the short-term mode with the rationale as applied to claim 1 above.

Regarding claim 17, Ishiwata discloses everything claimed as applied above. Dosho discloses wherein in the short-term mode, the positive input end of the operational amplifier is coupled to a reference voltage, and the negative input end thereof is coupled to the output end for forming a voltage follower so as to initialize the write-control signal (3, fig. 4). The rationale follows as in claim 1 above.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwata et al (US 6792013) in view of Dosho (US 5822236) as applied to claims 1-5, 8, 15-19 and 22 above, and further in view of Inaba et al (US 5477557).

Regarding claims 6-7 Ishiwata in view of Dosho fail to disclose a sampling and holding circuit and a gain amplifier, in which the sampling and holding circuit receives the feedback control signal and the feedback control signal is amplified by the gain amplifier, and the feedback control signal is amplified before being sent to the negative input end of the operational amplifier. In the same field of endeavor, Inaba discloses a laser drive circuit wherein a feedback signal is provided to the driving amplifier circuit through a gain amplifier and a sample and hold circuit (fig. 6). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the device disclosed by Iswhiwata in view of Dosho by providing a gain amplifier and sample and hold circuit as taught by Inaba. The rationale is as follows: One of ordinary skill in the art at the time of the applicant's invention would have been motivated to provide a gain amplifier and sample and hold circuits in order to a stable and detectable feedback signal from the photo-detector.

Response to Arguments

Applicant's arguments filed 1/29/2007 have been fully considered but they are not persuasive. Regarding applicant's arguments that Ishiwata fails to disclose using the "virtual ground effect" to charge the write control signal, this argument is not persuasive because Ishiwata discloses the same connections for an opaamp for charging the signal as disclosed by applicant. In Ishiwata during the long term mode, or charge up mode, the switch C2 is set to 1, which connects the output terminal with the negative input terminal of the opamp, while the

switch C0 is set to 1 such that the output of the D/A converter is applied to the positive input end, as acknowledged by applicant creating a voltage follower circuit (see applicant's argument on page 8 lines 17-21 and page 10 lines 18-21). Applicant then asserts that Ishiwata does not disclose providing a voltage follower circuit that charges the write control signal using a virtual ground effect. It is unclear what applicant is referring to with respect to the virtual ground effect. The disclosure of applicant's invention shows the long-term m ode in figure 7 with the "virtual ground effect," and the connections in that figure and the corresponding disclosure show the negative output of the amplifier tied the output of the opamp, while the positive terminal is connected to a D/A converter through an amplifier. The circuit disclosed by applicant is a voltage follower that charges the output terminal to reach the voltage input by the D/A converter to the positive input end due to the nature of an opamp circuit to have no effective current flowing into the terminals, resulting in the same voltage at the positive and negative input leads. The "virtual ground effect" claimed by applicant is interpreted to mean the property of an opamp when it is connected as a voltage follower to have the positive and negative input terminals effectively as the same voltage levels, which is disclosed by Ishiwata.

Regarding applicant's argument that Ishiwata in view of Dosho fail to disclose providing a voltage follower in the short term mode for initializing the write control signal, this argument is acknowledged but is not persuasive. Ishiwata does not disclose providing the voltage follower for the short-term initialization, and Dosho discloses providing a voltage follower circuit for initializing or grounding a circuit at the output. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413,

208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tawfik Goma whose telephone number is (571) 272-4206. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T. Goma
4/20/2007

WILLIAM KORZUCH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600